Notice of Allowability	Application No.	Applicant(s)	
	10/789,646	VENKATESWARAN, MUTHIAH	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt of 8/22/05*.

2. ☒ The allowed claim(s) is/are *20-30*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Drawings

1. The drawings were received on 11, October 2005. These drawings are approved by the Examiner.

Allowable Subject Matter

2. Claims 20-30 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The primary reason for allowance is the claimed combination of a layer of conductive material formed on the top of the package substrate and including both contact pads and a plate spaced apart from the contact pads and having the same height as the contact pads, wherein an underfill layer is disposed over both the plate layer and the contact pads.

The prior art of record, such as U.S. Patent No. 6,800,947 to Sathe, US 6,521,530 to Peters, or US 6,388,207 to Figueroa et al. can be construed as having the layer of conductive material including the contact pads and plate layer, there is no suggestion of the application of an underfill layer disposed between the semiconductor device and package substrate. Although insulating underfill materials are extremely well known in the art, and are frequently applied between semiconductor chips and package substrates in order to relieve thermal expansion or solder joint stresses, such underfill layers are generally only applied directly between the chip and the package substrate, such that the contact pads are surrounded. Hence, in order to meet the limitation of claims 20 and 29, which require that the underfill layer be disposed over the plate

layer, one would need to modify the prior art packages such that the underfill is either laterally extended out from the sides of the chip and across the package substrate, or one would need to reconfigure the plate layer portions such that they are interspersed with the chip contacts. There is further no suggestion in the prior art that the plate layer and contact pads have the same thickness.

Since the prior art does not fairly teach or suggest disposing an underfill material such that it covers both the contact pads and a metal plate layer, the pads and the plate layer having the same thickness, and since these claimed limitations yield the unexpected result of inhibiting crack propagation from the underfill layer into the package substrate (see paragraphs 0038 and 0039 of the Specification of the present application), it is the Examiner's opinion that the claimed invention is well beyond the purview of a person skilled in the art.

The Examiner further notes that US 2004/0036179 to Chiu, uses plate layers spaced apart from contact pads in order to inhibit crack propagation from an underfill layer into a package substrate, in a manner substantially similar to that disclosed by the Applicant. Chiu, however, does not constitute prior art (filing date of 8/23/02) and is merely cited as being of interest to the Applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

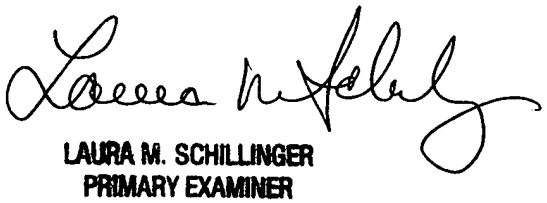
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd



LAURA M. SCHILLINGER
PRIMARY EXAMINER